AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("__") and the language being deleted contains either a strikethrough ("—") or is enclosed by double brackets ("[[ ]]").

LISTING OF CLAIMS

1-14. (Canceled)

15. (Currently Amended) A transmission signal integrity supervisor within an analog front end (AFE), wherein the transmission signal integrity supervisor is configured to detect anomalous conditions and protect the AFE, the transmission signal integrity supervisor comprising:

a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition, wherein the clock detector is further configured to forward the first output signal to at least one of control logic and devices external to the AFE; and

a data supervisor configured to receive a digital data stream and generate a second output signal in response to an at least one digital data stream anomalous condition, wherein the data supervisor is further configured to forward the second output signal to at least one of a line driver within the AFE and devices external the AFE.

16. (Original) The signal integrity supervisor of claim 15, wherein the first output signal is a reset signal.

17. (Original) The signal integrity supervisor of claim 15, wherein the second output signal is a power down signal.

18. (Original) The signal integrity supervisor of claim 15, wherein the data supervisor receives a digital data stream from a delta-sigma modulator.

19. (Currently Amended) The signal integrity supervisor of claim 15, wherein the clock detector comprises a first monostable circuit and a second monostable circuit.

20. (Original) The signal integrity supervisor of claim 19, wherein the clock detector further comprises: a current mirror; and a resistor-capacitor combination having a resistance and a capacitance value respectively, selected such that the first output signal triggers in response to a clock signal input that falls below a minimum frequency.

21. (Original) The signal integrity supervisor of claim 15, wherein the data supervisor comprises: a comparator; and a maximum number counter.

22. (Original) The signal integrity supervisor of claim 21, wherein the comparator is configured to compare a data value from a previous clock cycle with a current data value and to generate a reset signal in response to consecutive data levels that vary.

23. (Currently Amended) The signal integrity supervisor of claim 2[[1]]2, wherein the maximum number counter is configured to increment upon detecting a clock cycle until it receives the reset signal from the comparator.

24. (Original) The signal integrity supervisor of claim 23, wherein the maximum number counter is configured to generate an output signal upon reaching a maximum count.

25. (Original) The signal integrity supervisor of claim 24, wherein the maximum number counter comprises a 4-bit asynchronous counter.

26. (Currently Amended) A circuit, comprising:

means for monitoring a digital data stream, wherein the means for monitoring a digital data stream comprises a signal integrity supervisor; and

means for generating an output signal in response to an anomalous condition in the digital data stream, wherein the means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value.

27. (Original) The circuit of claim 26, wherein the anomalous condition in the digital data stream [[would]] creates a direct current (DC) transmit signal.

28. (Canceled)

29. (Currently Amended) The circuit of claim [[28]]26, wherein the signal integrity supervisor comprises a clock detector and a data supervisor.

30. (Canceled)

31. (Currently Amended) The circuit of claim [[28]]26, wherein the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency.

32. (Currently Amended) A transmission unit, comprising:

a signal integrity supervisor configured to generate a response to a digital data stream having an anomalous condition, the signal integrity supervisor further configured to forward the response to at least one of:

control logic capable of resetting the transmission unit,

a line driver within the transmission unit, wherein the response powers down the line driver, and

devices external to the transmission unit.

33. (Original) The transmission unit of claim 32, wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value.

34. (Original) The transmission unit of claim 32, wherein the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles.